VIDEO DECODER WITH SCALABLE ARCHITECTURE

Abstract of the Disclosure

A scalable architecture for a video decode system is provided for facilitating decoding of an encoded stream of video frames, such as a high definition (HD) bitstream. The architecture comprises multiple decoders connected in parallel to receive the encoded stream of video frames. Each decoder selects and decodes a respective portion of each frame of the bitstream, wherein cumulatively the respective portions decoded by the multiple decoders constitute the entire frame. In one embodiment, the decoders are standard definition (SD) decoders.